Logic Synthesis for FSM-Based Control Units: 53 (Lecture Notes in Electrical Engineering)

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The control unit is one of the most important parts of any digital system responsible for interplay of other system blocks. Very often, the model of a finite state machine (FSM) is used to represent the behaviour of a control unit. Modern computer-aided design tools include a lot of optimal solutions (library cells) for implementation of such regular blocks of digital systems as decoders, multiplexers, parallel multibit adders and so on. But as a rule, control units have an irregular structure which makes impossible to design their logic circuits using the standard library cells. To use these cells, an FSM can be represented by a multilevel model based on the principle of structural decomposition. In multilevel models, for example, multiplexers are used to replace logical conditions, decoders are used to implement microoperations, and different memory blocks are used to transform object codes. Design methods depend strongly on such factors as an FSM model in use, specific features of logic elements implementing its logic circuit, characteristics of a control algorithm to be interpreted. In the case of Moore FSM, optimization methods are based on existence of the classes of pseudoequivalent states. Their use permits to compress the transition table of Moore FSM till the size of the table for equivalent Mealy FSM. In the case of Mealy FSM, optimization methods are based on transformation of either object codes, or interpreted graph-schemes of algorithm. In the case of CPLD, the hardware decrease can be achieved using more than single source of state codes. In the case of FPGA, the structural decomposition allows using embedded memory blocks for implementation of decoding logic. In case of ASIC, design methods target on minimization of the chip area occupied by an FSM circuit. It can be achieved due to use of different encoding methods, where both internal states and collections of microoperations can be encoded. If a control algorithm is a linear one, then a state register of Moore FSM can be replaced by a counter. It leads to simplification of the input memory functions and, in turns, to the hardware amount decrease. The book includes a lot of design methods targeted on logic synthesis of both Mealy and Moore FSMs, where their logic circuits can be implemented using ASIC, as well as CPLD or FPGA. The most of discussed methods belong to the authors of this book. This book will be interesting and useful for students and postgraduates in the area of Computer Science, as well as for designers of digital systems included complex control units. Proposed models and design methods open new possibilities for creating logic circuits of control units with optimal hardware amount.

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